REMARKS

The Applicants request reconsideration of the rejection. Claims 1-12 are pending.

The Examiner has objected to the claims as set forth on page 2 of the Office Action. Specifically, the Examiner finds an inconsistency between the description of the phase-locked loop in claim 2 and the "path separate from the path of said phase-locked loop" in claim 3; and an unclarity in the scope of the method of claim 10 with regard to the device of claim 1.

Regarding claims 2 and 3, the Applicants note that claim 2 states that the voltage-controlled oscillation circuit, phase comparison circuit, and control voltage generation circuit form a phase-locked loop (see, for example, Figure 3 (VCO 134, phase comparator 137, and charge pump 138)), whereas claim 3 recites that the second control voltage (for example, Vcnt2) is supplied to the voltage-controlled oscillation circuit separate from the path of the phase-locked loop, as also shown in Figure 3 (the second control voltage is output from low pass filter 133 in Figure 3). Thus, the Applicants believe that there is no indefiniteness or other error requiring correction in claims 2 or 3.

Regarding claims 10 and 1, the method of claim 10 is a method of testing a semiconductor integrated circuit device including the limitations set forth therein. Claim 10 has no dependency on claim 1 and should be examined independently. Further, because claim 1 is directed to a device and not an apparatus, the Applicants do not understand the Examiner's assumption that the method of claim 10 "is read out from the apparatus of claim 1." Nevertheless, it is believed that the amendments to claims 10 clarify the recited method.

Claims 1-3, 5, 6, and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chaplik et al U.S. Patent No. 5,412,353 (Chaplik). Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Chaplik in view of Zuta et al U.S. Patent No. 6,016,080 (Zuta).

The Applicants respectfully traverse these rejections, specifically addressing deficiencies in Chaplik that are found neither in Zuta nor in the other prior art of record. Specifically, the prior art is not seen to disclose or fairly suggest the modulation semiconductor integrated circuit device in which a modulation frequency deviation of the voltage-controlled oscillation circuit due to so-called "frequency hopping" is reduced by controlling a reference current in accordance with the changing carrier frequency.

Chaplik discloses a phase-locked loop frequency modulation circuit for use in, for example, a cellular telephone apparatus, which has the objective of compensating for the inability of prior phase-locked loop circuits to pass low-frequency content of an input modulation signal. To this end, Chaplik employs a compensation circuit that receives an input modulation signal, and integrates and filters the input modulation signal before adding back the input modulation signal to provide a compensation signal 78, which is added to a loop filter output signal 70 of the phase-locked loop circuit to provide a control signal 62 to the input of the voltage-controlled oscillator 40 of the phase-locked loop circuit.

Thus, Chaplik does not disclose the claimed device or method in which the voltage-controlled oscillation circuit is arranged to receive a first control voltage to produce a carrier frequency signal, and a second control voltage to produce a modulation frequency signal, wherein the carrier frequency "hops" by changing the first control voltage. Further, Chaplik does not teach or suggest the claimed circuit for producing the second control voltage, having a reference current value controlled in response to the change of the carrier frequency such that the variation of the second

control voltage in response to the carrier frequency change exhibits a characteristic that is opposite to the characteristic of modulation frequency deviation of the voltage-controlled oscillation circuit. In other words, Chaplik has a different structure than that of the claimed invention, and does not perform a testing method in which the modulation frequency deviation is reduced.

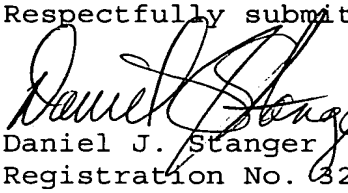
As set forth in the Summary of the Invention, the present inventors have found that the adoption of frequency modulation based on direct control of an LC-oscillation voltage-controlled oscillation circuit is problematic in that the switching of carrier frequency ("hopping") causes the frequency deviation. For example, the Bluetooth protocol recommends a modulation range of ± 140-175 kHz for the transmission of a signal having a 2.4 GHz carrier signal rendered with ± 160 kHz modulation. In other words, the protocol allows a margin of 35 kHz.

The inventors have found that, when attempting to modulate the carrier signal at a constant level in accordance with the transmission data (i.e., when attempting to control the oscillation frequency of the VCO at a constant level of control voltage irrespective of the carrier frequency), frequency hopping causes the variation of not only the

capacitance of the varactor diode pair Dv11 and Dv12, but also the total capacitance of another varactor diode pair Dv21 and Dv22 (see Figure 2). It was thus revealed that the frequency variation caused by the variation of the total capacitance resulting from carrier frequency hopping varies the modulation gain of the VCO, causing the modulation frequency to deviate with the carrier frequency as shown in Figure 7A. Specifically, a 10% variation between the high and low limits of the VCO oscillation frequency due to modulation gain results in a loss of as much as 16 kHz of the 35 kHz frequency margin due to the frequency hopping, leaving a practical frequency margin of less than 20 kHz. It is the reduction of this modulation frequency deviation that is achieved by the present invention.

In view of the foregoing amendments and remarks, the Applicants request reconsideration of the rejection and allowance of the claims.

Respectfully submitted,



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